

FIG. 1A

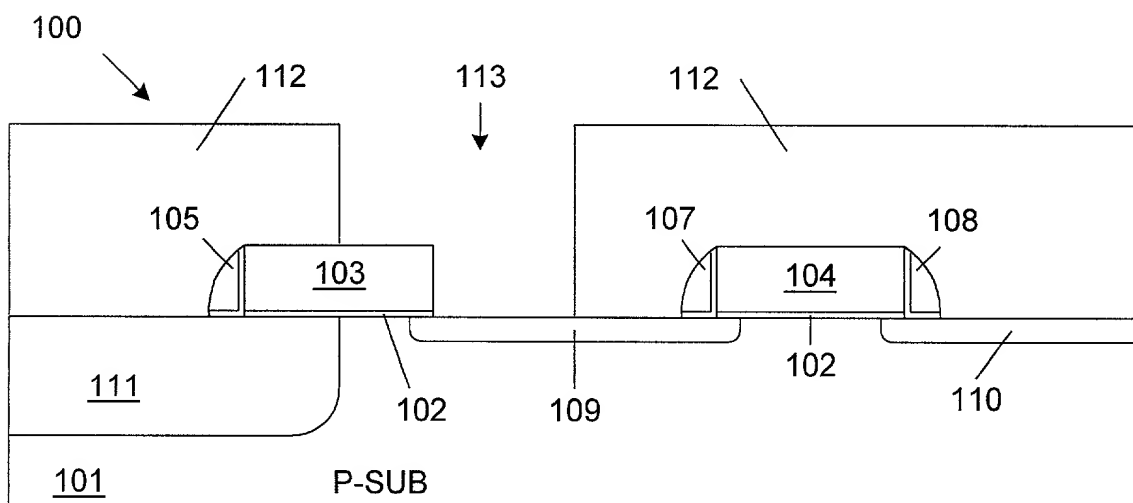


FIG. 1B

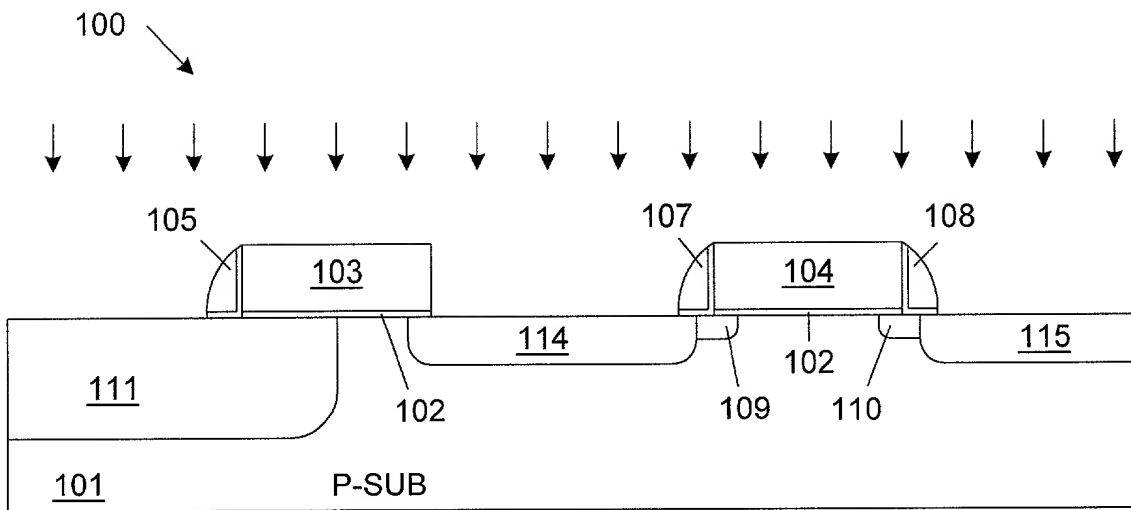


FIG. 1C

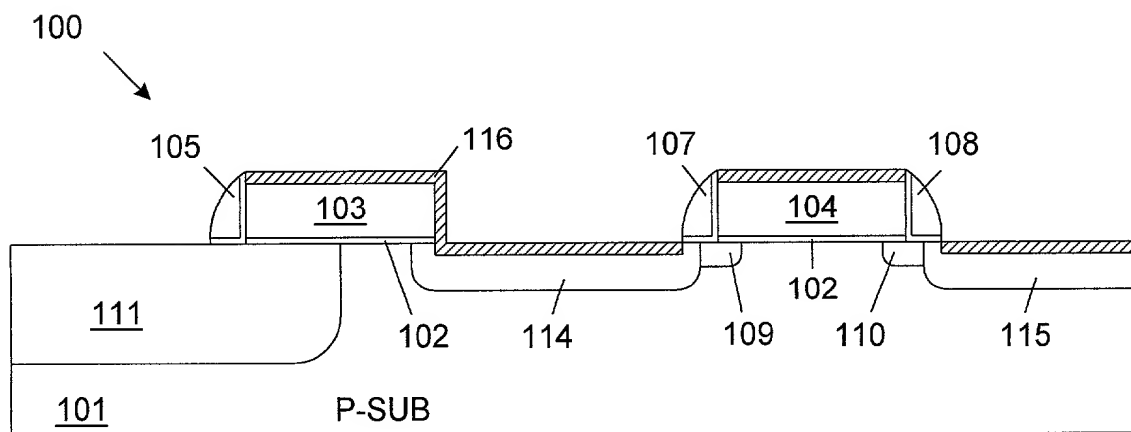


FIG. 1D

A cross-sectional view of a semiconductor device. A substrate 201 is labeled "P-SUB". A layer 202 is on top of the substrate. Two gate electrodes, 204 and 205, are on top of layer 202. Gate electrode 204 is connected to a terminal 200. Gate electrode 205 is connected to a terminal 213. The regions between the gate electrodes are labeled 206, 207, 208, and 209. The regions under the gate electrodes are labeled 210, 211, and 212. The regions 210, 211, and 212 are labeled "N".

A cross-sectional view of a semiconductor device. It features a P-SUB (P-type substrate) at the bottom, labeled 201. Two N-type regions, 210 and 212, are formed in the substrate. Two gates, 202 and 203, are positioned on top of the substrate. Gate 202 is wider than gate 203. A channel region 204 is located between the two gates. A second channel region 205 is located under gate 203. A layer 206 is on top of gate 202, and a layer 207 is on top of gate 203. A layer 208 is on top of the substrate between the gates. A layer 209 is on top of the substrate to the right of gate 203. A layer 211 is on top of the substrate to the left of gate 202. A layer 213 is on top of the substrate to the right of gate 203. A layer 214 is on top of the substrate to the left of gate 202. A layer 215 is on top of the substrate to the right of gate 203. The width of gate 202 is 0.1 μm, and the width of gate 203 is 0.15 μm.

FIG. 2C

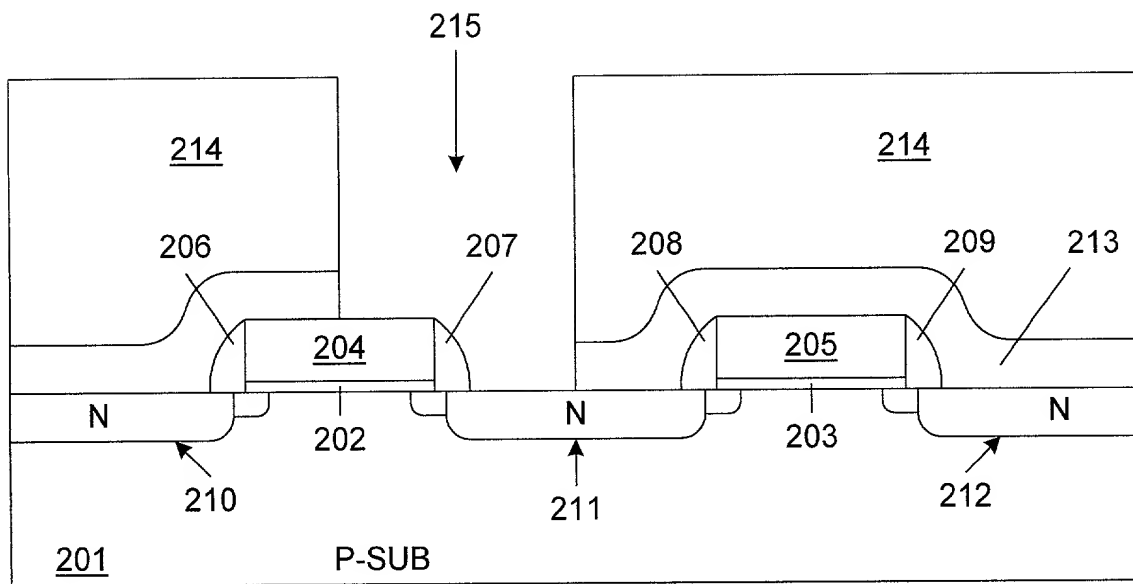


FIG. 2D

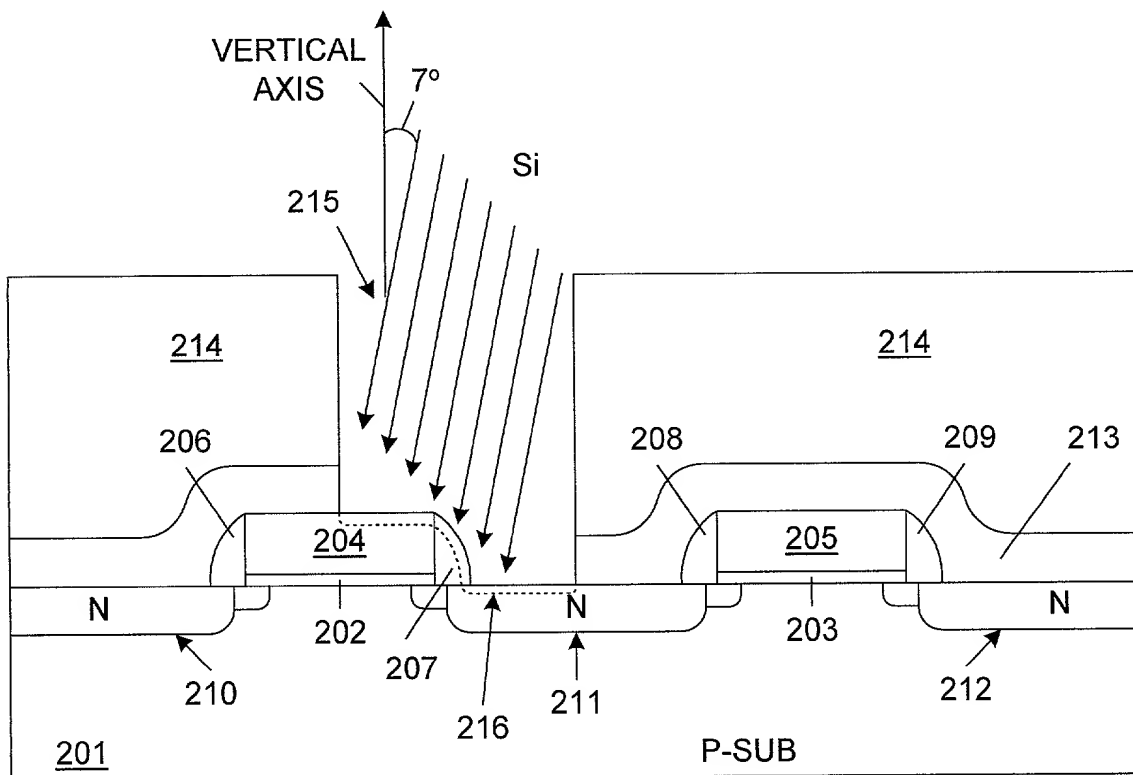


FIG. 2E

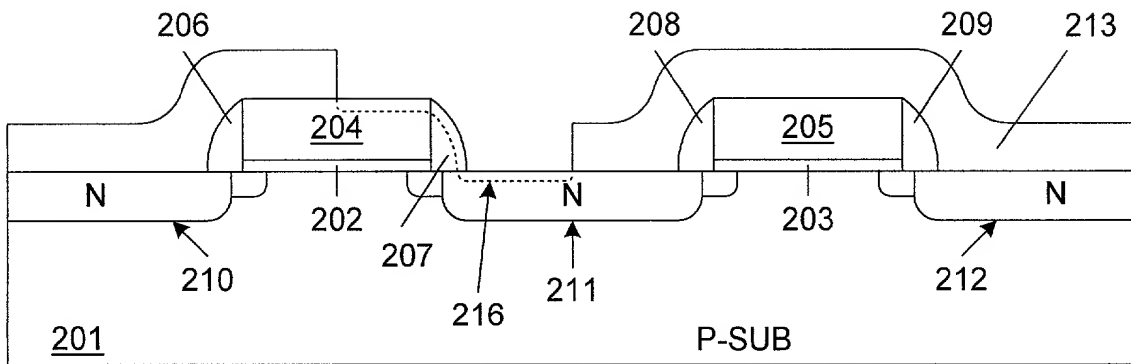


FIG. 2F

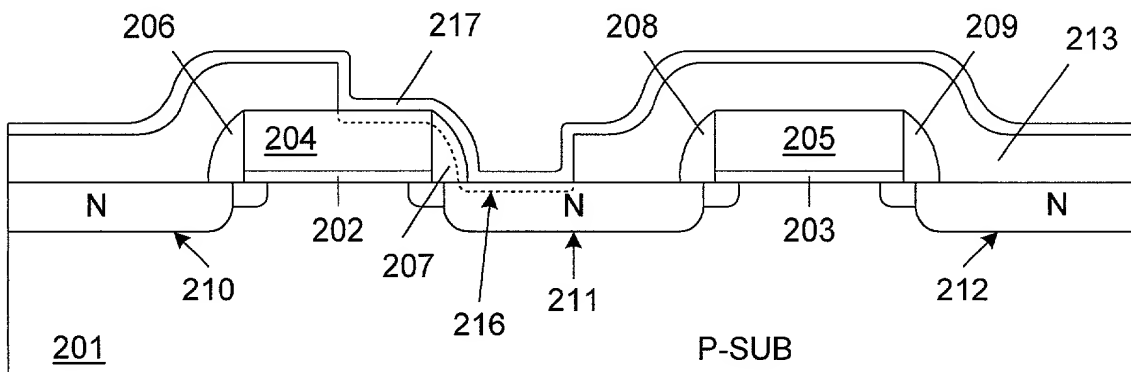


FIG. 2G

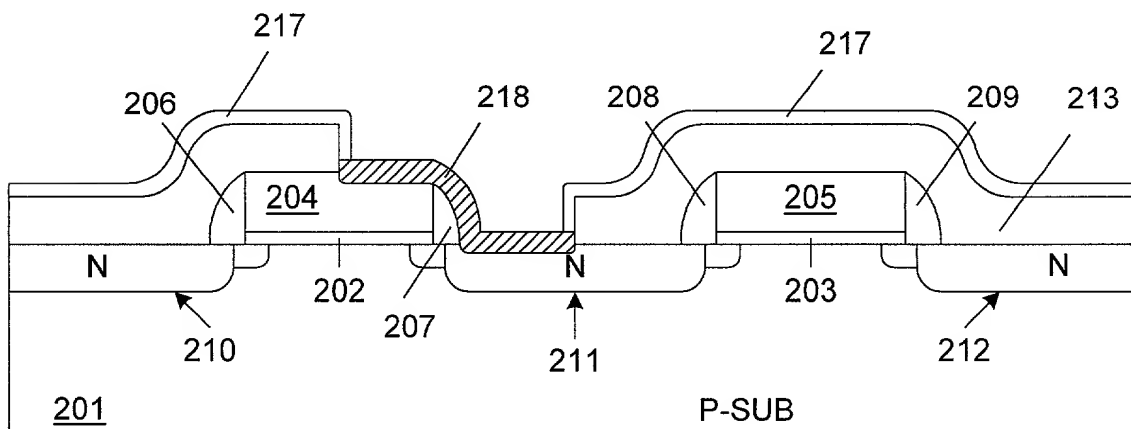


FIG. 2H

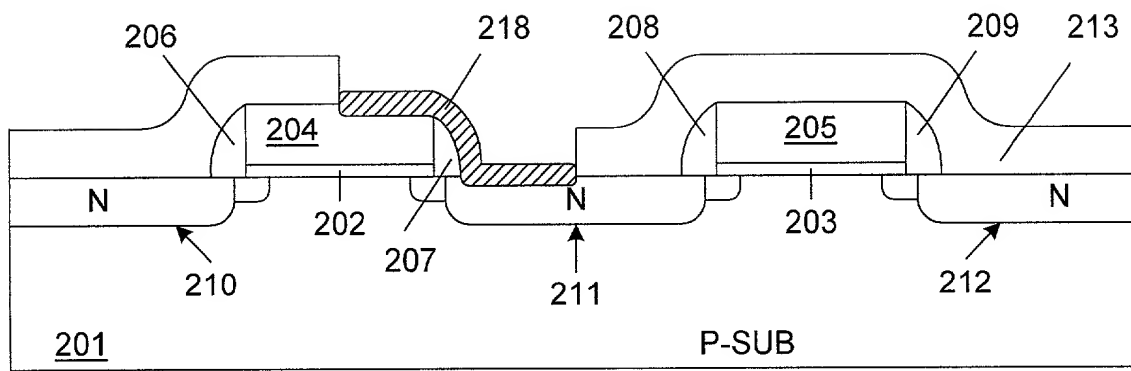


FIG. 2I